5E 5022

5E 5022

B. Tech. V Semester (Main/Back) Examination, Dec., 2014

ELECTRONICS & COMMUNICATION ENGG. # 5EC2A

LINEAR INTEGRATED CIRCUITS

Time : 3 Hours **Min. Passing Marks : 24** **Maximum Marks : 80**

Instruction to Candidates :

*Attempt any **five** questions, selecting **one** question from **each** unit. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.)*

Unit–'I'

1. (*a*) The following specifications are given for the dual input, balanced output bipolar differential amplifier:
$R_C = 2.2\ k\Omega$, $R_E = 4.7k\Omega$, $R_S = 50\Omega$, $V_{CC} = 10V$, $V_{EE} = -10V$ and $\beta_F = \beta_0 = 100$. Assume $V_{BE} = 0.7V$. Find:
(i) I_{CQ} and V_{CEQ}
(ii) Differential-mode voltage gain φ
(iii) Input and output resistances. |10|

(*b*) For Fig. (1):
$R_1 = R_2$, Slew rate = 50V/MS, $S_i = 10 \sin wt$
Find f_{max} for undistorted output.

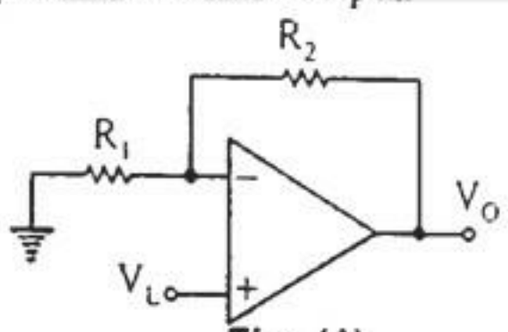

Fig. (1) |6|

OR

1. (*a*) A Bipolar differential amplifier uses a BJT having $\beta_0 = 200$ and biased at I cφ = 100 MA. Determine R_C and R_E so that $/ A_{dm} / = 500$ and CMRR = 80 dB. |10|

(*b*) Draw only output waveform with voltage level for fig. (2):
$V_Z = 5.1V$, $V_D = 0.7V$, supply = ±15V

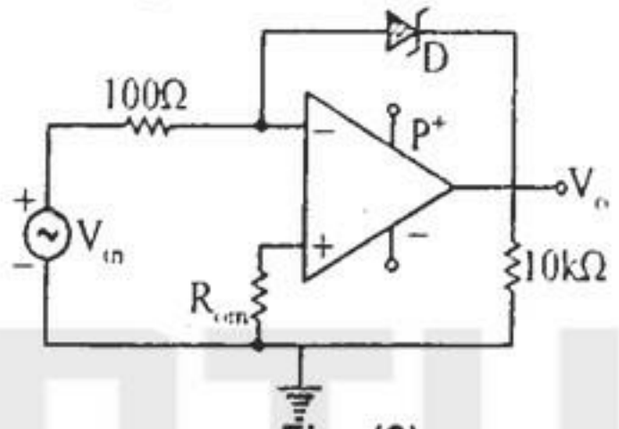

Fig. (2) |6|

Unit–'II'

2. (*a*) Draw only circuit diagram of a square wave oscillator and design it for:
f_0 = 1 kHz using 741ϕ, supply = ± 15V |8|

(*b*) Draw the circuit diagram and explain the working of a voltage controlled-oscillator. |8|

OR

2. Design the following and also draw the - circuit diagrams of:
(a) Wein bridge oscillator - f_0 = 2 KHz, amplifier's grin = 5 |8|
(b) Phase shift oscillator - f_0 = 2KHz, amplifier's gain = 32 |8|

Unit–'III'

3. Explain first and second - order switched capacitor filters with required circuits. Also find relations between f_0, f_{CLK} and capacitors. Mention the effect of stray capacitances and how stray capacitance errors can greatly reduce. |16|

OR

3. (*a*) Draw and explain twin-T narrow band reject filter (Notch filter). |8|

(*b*) Design a second-order low pass Butterworth filter (Takes care of guaranteed Butterworth response) for a cutoff frequency of 2 kHz. Also draw the circuit diagram. |8|

Unit–'IV'

4. (*a*) Explain following with required diagram and waveforms using multiplier.
(i) Frequency doubling. |4|
(ii) Square root. |4|

(*b*) Draw and explain 555 as table multi-vibrator. |8|

OR

4. Draw the output waveform and explain the working of fig. (3) and fig. (4).

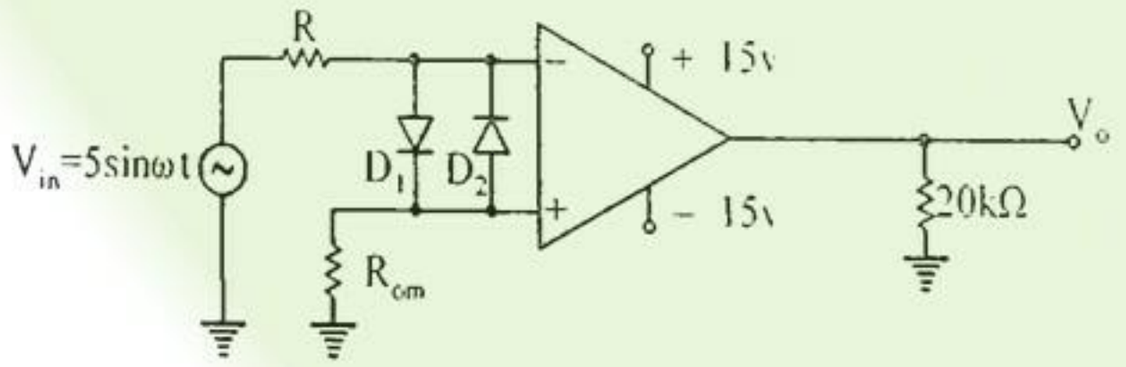

Fig. (3)

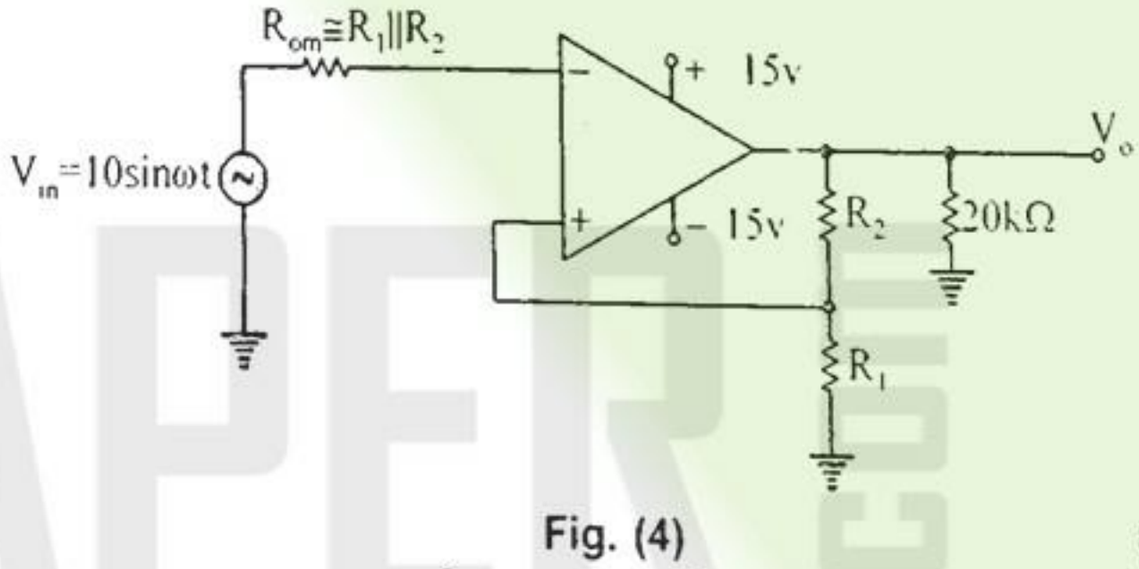

Fig. (4) |6|

Unit–'V'

5. (*a*) Draw and explain the working of an Antilog amplifier using diode. |8|

(*b*) A PLL has a VCO with K_0 = 20 kHz/V and f_C = 50 kHz. The amplifier gain is A = 2 and the phase detector has a maximum output voltage swing of ± 0.7V. Find the lock range of the PLL. Assume gain equal to unity. |8|

OR

5. (*a*) Draw the block diagram of PLL and explain working in detail. |10|

(*b*) Explain FSK demodulator using PLL. |6|