7E4048

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B. Tech. VII Semester (Main/Back) Examination 2013

ELECTRONICS & COMMUNICATION # ⑦EC⑤

VLSI DESIGN

Time : 3 Hours **Min. Passing Marks : 24** **Maximum Marks : 80**

Instruction to Candidates :

*Attempt any **five** questions, selecting **one** question from **each** unit. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.)*

Unit-'I'

1. (*a*) What are the types of MOSFETs. Draw the schematic diagrams and circuit symbols for all. [4]
   (*b*) Explain the operation of enhancement NMOS using suitable diagrams. [9]
   Also draw the characteristics and justify that it is a voltage controlled current device after seeing the characteristics. [3]

OR

1. (*a*) Explain the NMOS fabrication process with the help of neat diagrams. [8]
   (*b*) Write the steps to fabricate n-well CMOS (NOT the diagrams). [3]
   (*c*) Write a short note on "depletion mode MOSFET". [5]

Unit-'II'

2. (*a*) Derive $I_{ds} - V_{ds}$ relationship for MOSFET. [8]
   Also prove that the drain current $I_D = C(1 + \lambda V_{DS})$ in case of channel length modulation. Where $C = \frac{1}{2}K'_n\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$, λ = process technology parameter. [4]
   (*b*) The NMOS device with $V_t = 0.7V$ has its source terminal grounded and a 1.3v is applied to gate. The device has μ_n, $C_{ox} = 100\ \mu A/V^2$, W = 10 μm, L = 1μm. Find the value of drain current for $V_D = 3V$. [4]

OR

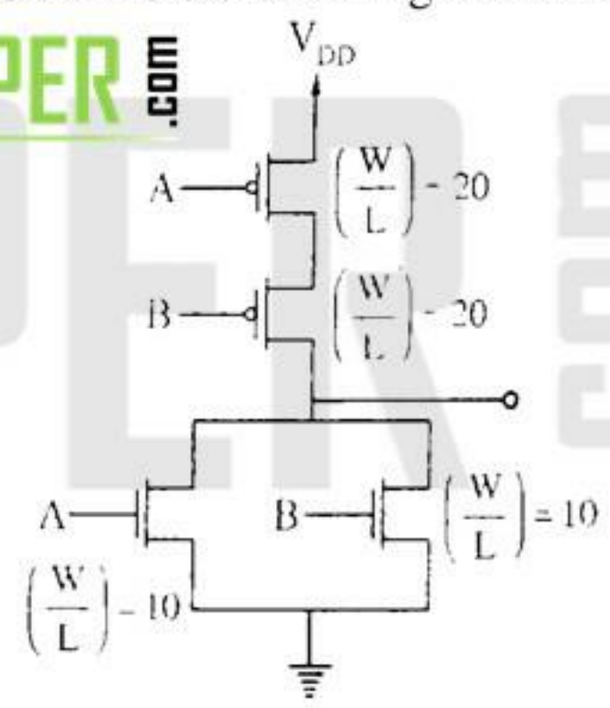
2. (*a*) Prove that the pull-up to pull-down ratio for a NMOS inverter is 4:1 when it is driven by another inverter. [8]
   (*b*) Derive the β_n/β_p ratio of a CMOS Inverter. [8]

Unit-'III'

3. (*a*) Implement clocked S-R Flip-Flop using CMOS Inverter. [8]
   (*b*) Explain transistor sizing of CMOS. [5]
   (*c*) Implement OR gate using transmission gate. [3]

OR

3. (*a*) Realize the following logic expression using CMOS Inverter:
   (*i*) $A.B + \bar{A}.\bar{B}$
   (*ii*) $A.B.\bar{C} + \bar{A}.B.C$
   (*iii*) $A.B.\overline{C.D}$
   (*iv*) $AB + BC + AC$
   (*b*) Find the equivalent (W/L) ratio of NMOS and PMOS transistors in the given CMOS circuit. [6]



Unit-'IV'

4. (*a*) Draw the stick diagrams of
   (*i*) 3 i/p NAND gate
   (*ii*) 3 i/p NOR gate [4+4=8]
   (*b*) Write a short note on "Layout optimization for performance". [8]

OR

4. (*a*) Draw the stick diagram and layout for the following boolean expression Y = A.B + C.D + E [8]
   (*b*) What is "Euler path"? What is use of it? Explain with a suitable example. [8]

Unit-'V'

5. (*a*) What do you meant by VHDL ?
   Write a VHDL code for
   (*i*) Full Adder
   (*ii*) J-K Flip-flop [2+4+4=10]
   (*b*) Distinguish between
   (*i*) Signal and variable [3]
   (*ii*) Concurrent and sequential Assignment. [3]

OR

5. (*a*) Write a VHDL code for: [8]
   (*i*) S-R Flip-Flop.
   (*ii*) 4 bits adder using full adder.
   (*b*) Explain:
   (*i*) Entity declaration [2]
   (*ii*) Behavioral style of modelling [3]
   (*iii*) Structural style of modelling [3]