

7E7034

Roll No. \_\_\_\_\_

Total No of Pages: 2

7E7034

B. Tech. VII Sem. (Main/Back) Exam., Nov.-Dec.-2016

Computer Science & Engineering

7CS4A Computer Aided Design for VLSI

Time: 3 Hours

Maximum Marks: 80

Min. Passing Marks Main : 26

Min. Passing Marks Back: 24

Instructions to Candidates:

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.

(Mentioned in form No. 205)

1. NIL

2. NIL

### UNIT - I

Q.1 (a) Discuss classes of computational complexities in increasing order of time. [6]

(b) Explain VLSI simple design cycle [10]

OR

Q.1 Discuss various VLSI design automation tools in physical design cycle. [16]

### UNIT - II

Q.2 Explain how ROBDD is used in logic synthesis. [16]

OR

Q.2 Discuss breadth-first search algorithm with the help of suitable example. [16]

[7E7034]

Page 1 of 2

[6040]

**UNIT – III**

Q.3 Discuss resource constrained scheduling algorithm with all its assumptions. Take suitable example to demonstrate. [16]

**OR**

Q.3 Discuss following scheduling with the help of suitable diagrams-

(a) ASAP [8]

(b) ALAP [8]

**UNIT – IV**

Q.4 Discuss Quine - McCluskey algorithm for two-level logic minimization problem. [16]

**OR**

Q.4 Write short notes on following -

(a) Binding Variable to Registers [8]

(b) Functions with Multivalued Logic [8]

**UNIT – V**

Q.5 Explain 'Floor plan of Order 5'. [16]

**OR**

Q.5 Write short notes on following -

(a) Clock Planning [8]

(b) Goals & Objectives of Global Routing [8]