7E7034

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B.Tech. VII Semester (Main) Examination, Dec. - 2015

Computer Science & Engineering

7CS4A Computer Aided Design for VLSI

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 24

Instructions to Candidates:

*Attempt any **five** questions, selecting one question from **each unit**. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.)*

Unit - I

1. a) What are the different semi-custom design styles for circuits? **(8)**

b) Explain the four phases in creating micro electronics chips in computer aided synthesis and optimization. **(8)**

OR

1. a) What are the various views and levels of the micro electronic circuit models. Also express the relation between them. **(8)**

b) Compare the following task realization approaches:

i) Full custom

ii) Semi custom.

iii) Off the shelf IC package

iv) Off the shelf micro computer. **(2×4=8)**

Unit - II

2. a) What is Binary decision diagram? Explain ROBDD algorithm. **(8)**

   b) Explain the compilation and behavioral optimizations. **(8)**

OR

2. a) Explain ITE algorithm and QUANTIFY algorithm. **(8)**

   b) Write short note on:

      i) Abstract models

      ii) Hierarchical sequencing graphs. **(4×2=8)**

Unit - III

3. a) Explain ASAP scheduling algorithm using one example. **(8)**

   b) Distinguish between temporal and spatial domain scheduling. Give one example explaining resource binding in hierarchical sequencing graph. **(8)**

OR

3. a) Explain Heuristic scheduling algorithm with example, show optimum schedule under resource constraints. **(8)**

   b) Discuss the classification and categories of resource and constraints with the help of examples. **(8)**

Unit - IV

4. a) Explain resource sharing and resource binding. What are compatibility and conflict graphs? **(8)**

   b) Write the algorithm for exact logic minimization with an example. **(8)**

OR

4. a) Explain register sharing and bus sharing with the help of example. **(8)**

   b) State and explain the principles of logic optimization. **(8)**

Unit - V

5. a) Explain physical design cycle with appropriate diagram. **(8)**

   b) Explain Global routing along with goals and objectives. **(8)**

OR

5. a) Explain left edge algorithm with an example. **(8)**

   b) Explain clock routing, power routing and via minimization. **(8)**