5E3251

Roll No. _____ Total No. of Pages : 3

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B.Tech. V SEM (Main/Back) Examination Dec.2012

Computer Science

5CS1-Computer Architecture

Common Computer & IT

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 32

Instructions to Candidates:

*Attempt any **five questions.** Selecting one Question from each unit. All questions carries **equal** marks. Schematic diagram must be shown wherever necessary. Any feel suitable be assumed and stated clearly. Units of Quantities used/calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. **Nil** 2. **Nil**

UNIT-I

Q.1. (a) List at least five essential functional blocks that any computer should possess. Describe briefly the role of each block. (8)

(b) Define three state bus buffers. What do you understand by High Impedance state in three state buffers? (8)

OR

(a) Describe the Von-Newman Model & functioning. (8)

1. Memory address Register.
2. Instruction Register.
3. Program Counter.

(b) Draw 4-bit adder substractor circuit. Following are the values for input mode M and data input A and B. In each case determine the values of the outputs: S3, S2, S1, S0 and C4. (8)

	M	A	B
a	0	0111	0110
b	0	1000	1001
c	1	1100	1000
d	1	0101	1010
e	1	0000	0001

UNIT-II

Q.2. (a) What do you mean by instruction formats? What are its types? Explain . (8)

(b) Describe role of addressing modes used in computer. (8)

OR

(a) How pipeline processing is done in an instruction pipeline? Explain with timing diagram for four segment instruction pipeline. (8)

(b) What do you mean by parallel processing? Write the Flynn's classification of parallel processing. (8)

UNIT-III

Q.3. (a) Describe the procedure for addition and subtraction for fixed-point number? Explain it by use of Flowchart. (8)

(b) Divide (-12) by (-4) when these numbers represent in sign magnitude form. (8)

OR

(a) Draw and Explain flow chart for Hardware divide operation . (8)

(b) Explain hardware for signed-magnitude addition subtraction with block diagram. (8)

UNIT-IV

Q.4. (a) Explain associative memory with its hardware organization. Explain how the data is read and write in the associative memory. (8)

(b) Explain paging and segmentation with suitable example. (8)

OR

(a) What are the various mapping methods used with cache memory organization? Explain any one method in detail. (8)

(b) What is need of virtual memory in the computer System? Explain how the page map table is organized in virtual memory system. (8)

UNIT-V

Q.5. (a) Draw and explain the diagram of a DMA controller. Why read and write lines of DMA are Bidirectional. (8)

(b) What is the function IOP? Explain it with block Diagram. (8)

OR

(a) Explain Daisy Chaining Priority Interrupt. (8)

(b) Differentiate B/W memory mapped I/O and isolated I/O. What are the advantages and disadvantages of each. (8)
